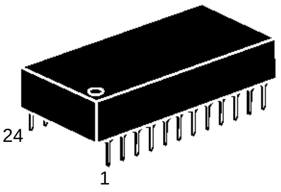
M48Z02
M48Z12

CMOS 2K x 8 ZEROPOWER SRAM

- INTEGRATED ULTRA LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT and BATTERY
- UNLIMITED WRITE CYCLES
- READ CYCLE TIME EQUALS WRITE CYCLE TIME
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- CHOICE of TWO WRITE PROTECT VOLTAGES:
  - – M48Z02: $4.5V \leq V_{PFD} \leq 4.75V$
  - – M48Z12: $4.2V \leq V_{PFD} \leq 4.5V$
- SELF CONTAINED BATTERY in the CAPHAT DIP PACKAGE
- 10 YEARS of DATA RETENTION in the ABSENCE of POWER
- PIN and FUNCTION COMPATIBLE with JEDEC STANDARD 2K x 8 SRAMs



PCDIP24 (PC)
Battery CAPHAT

DESCRIPTION

The M48Z02,12 ZEROPOWER® RAM is a 2K x 8 non-volatile static RAM which is pin and functional compatible with the MK48Z02,12.

A special 24 pin 600mil DIP CAPHAT™ package houses the M48Z02,12 silicon with a long life lithium button cell to form a highly integrated battery backed-up memory solution.

Table 1. Signal Names

A0-A10	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

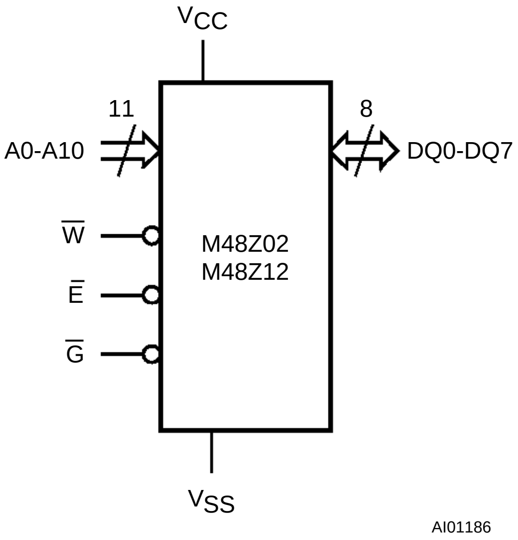


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature grade 1 grade 6	0 to 70 –40 to 85	°C
T_{STG}	Storage Temperature (V_{CC} Off)	–40 to 85	°C
V_{IO}	Input or Output Voltages	–0.3 to 7	V
V_{CC}	Supply Voltage	–0.3 to 7	V
I_O	Output Current	20	mA
P_D	Power Dissipation	1	W

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum ratings conditions for extended periods of time may affect reliability.

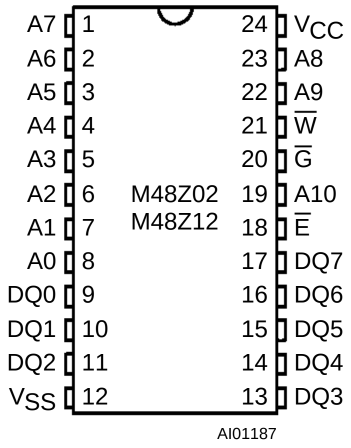
CAUTION: *Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.*

Table 3. Operating Modes

Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.75V to 5.5V or 4.5V to 5.5V	V_{IH}	X	X	High Z	Standby
Write		V_{IL}	X	V_{IL}	D_{IN}	Active
Read		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Read		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min)	X	X	X	High Z	CMOS Standby
Deselect	≤ V_{SO}	X	X	X	High Z	Battery Back-up Mode

Note: X = V_{IH} or V_{IL}

Figure 2. DIP Pin Connections



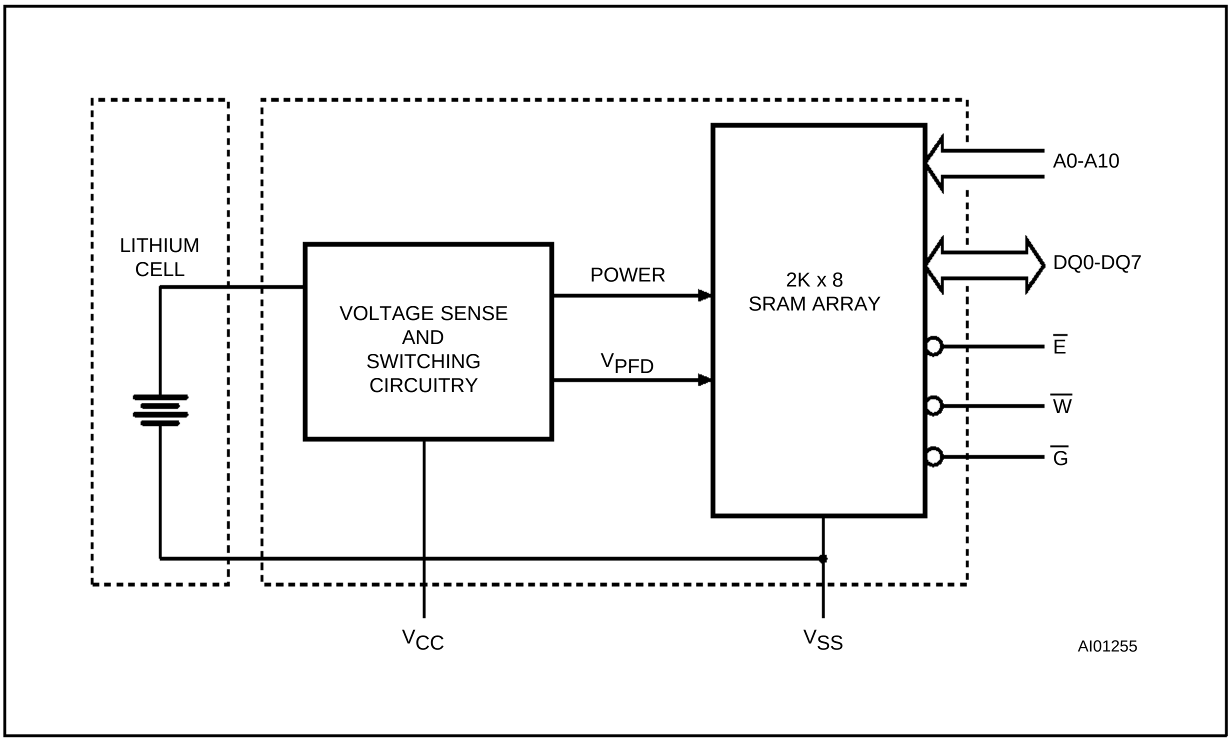
DESCRIPTION (cont'd)

The M48Z02,12 button cell has sufficient capacity and storage life to maintain data and clock functionality for an accumulated time period of at least 10 years in the absence of power over the operating temperature range.

The M48Z02,12 is a non-volatile pin and function equivalent to any JEDEC standard 2K x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The M48Z02,12 also has its own Power-fail Detect circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC}. As V_{CC} falls below approximately 3V, the control circuitry connects the battery which maintains data and clock operation until valid power returns.

Figure 3. Block Diagram



READ MODE

The M48Z02,12 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The device architecture allows ripple-through access of data from eight of 16,384 locations in the static storage array. Thus, the unique address specified by the 11 Address Inputs defines which one of the 2,048 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within t_{AVQV} (Address Access Time) after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the latter of the Chip Enable Access Time (t_{ELQV}) or Output Enable Access Time (t_{GLQV}).

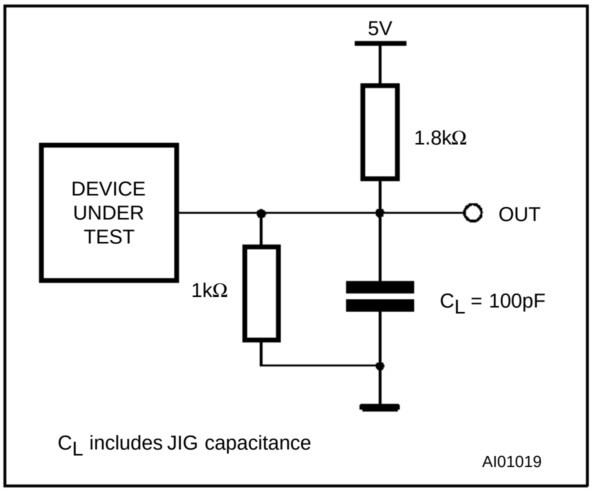
The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain active, output data will remain valid for t_{AXQX} (Output Data Hold Time) but will go indeterminate until the next Address Access.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0.6V to 2.4V
Input and Output Timing Ref. Voltages	0.8V to 2.2V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit



C_L includes JIG capacitance

Table 4. Capacitance [1] (T_A = 25 °C)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		10	pF
C_{IO} [2]	Input / Output Capacitance	V_{OUT} = 0V		10	pF

Notes: 1. Effective capacitance calculated from the equation C = IΔt/ΔV with ΔV = 3V and power supply at 5V.
2. Outputs deselected

Table 5. DC Characteristics (T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI} [1]	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		±1	µA
I_{LO} [1]	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$		±5	µA
I_{CC}	Supply Current	Outputs open		80	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		3	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} - 0.2V$		3	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V

Note: 1. Outputs Deselected.

Table 6. Power Down/Up Trip Points DC Characteristics [1] (T_A = 0 to 70°C or –40 to 85°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage (M48Z02)	4.5	4.6	4.75	V
V_{PFD}	Power-fail Deselect Voltage (M48Z12)	4.2	4.3	4.5	V
V_{SO}	Battery Back-up Switchover Voltage		3.0		V
t_{DR}	Expected Data Retention Time	10			YEARS

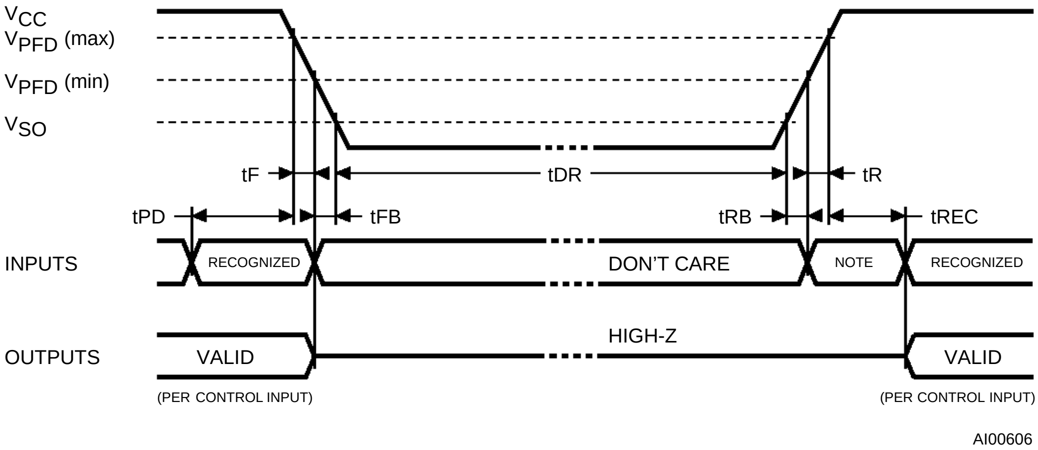
Note: 1. All voltages referenced to V_{SS}.

Table 7. Power Down/Up Mode AC Characteristics (T_A = 0 to 70°C or –40 to 85°C)

Symbol	Parameter	Min	Max	Unit
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0		µs
t_F (1)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB} (2)	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs
t_R	V_{PFD}(min) to V_{PFD} (max) V_{CC} Rise Time	0		µs
t_{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	1		µs
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} after Power Up	2		ms

Notes: 1. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 50 µs after V_{CC} passes V_{PFD} (min).
2. V_{PFD} (min) to V_{SO} fall time of less than t_{FB} may cause corruption of RAM data.

Figure 5. Power Down/Up Mode AC Waveforms



Note: Inputs may or may not be recognized at this time. Caution should be taken to keep $\overline{E}$ high as V_{CC} rises past V_{PFD}(min). Some systems may performs inadvertent write cycles after V_{CC} rises above V_{PFD}(min) but before normal system operations begins. Even though a power on reset is being applied to the processor a reset condition may not occur until after the system clock is running.

Table 8. Read Mode AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z02 / 12						Unit
		-120		-150		-200		
		Min	Max	Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	120		150		200		ns
t_{AVQV}	Address Valid to Output Valid		120		150		200	ns
t_{ELQV}	Chip Enable Low to Output Valid		120		150		200	ns
t_{GLQV}	Output Enable Low to Output Valid		75		75		80	ns
t_{ELQX}	Chip Enable Low to Output Transition	10		10		10		ns
t_{GLQX}	Output Enable Low to Output Transition	5		5		5		ns
t_{EHQZ}	Chip Enable High to Output Hi-Z		30		35		40	ns
t_{GHQZ}	Output Enable High to Output Hi-Z		30		35		40	ns
t_{AXQX}	Address Transition to Output Transition	5		5		5		ns

Figure 6. Read Mode AC Waveforms

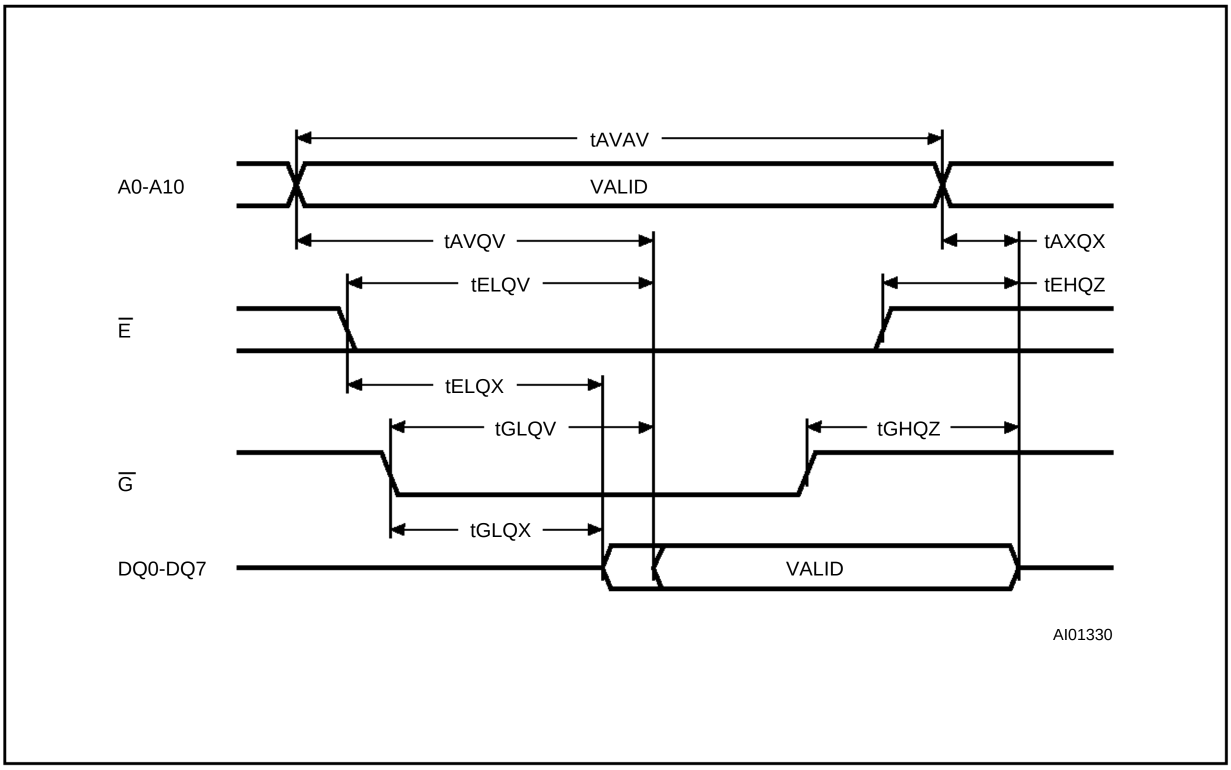


Table 9. Write Mode AC Characteristics
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	M48Z02 / 12						Unit
		-120		-150		-200		
		Min	Max	Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	120		150		200		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		0		ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		0		ns
t_{WLWH}	Write Enable Pulse Width	75		90		120		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	75		90		120		ns
t_{WHAX}	Write Enable High to Address Transition	10		10		10		ns
t_{EHAX}	Chip Enable High to Address Transition	10		10		10		ns
t_{DVWH}	Input Valid to Write Enable High	35		40		60		ns
t_{DVEH}	Input Valid to Chip Enable High	35		40		60		ns
t_{WHDX}	Write Enable High to Input Transition	5		5		5		ns
t_{EHDX}	Chip Enable High to Input Transition	5		5		5		ns
t_{WLQZ}	Write Enable Low to Output Hi-Z		40		50		60	ns
t_{AVWH}	Address Valid to Write Enable High	90		120		140		ns
t_{AVEH}	Address Valid to Chip Enable High	90		120		140		ns
t_{WHQX}	Write Enable High to Output Transition	10		10		10		ns

WRITE MODE

The M48Z02,12 is in the Write Mode whenever $\overline{W}$ and $\overline{E}$ are active. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for minimum of t_{EHAX} from Chip Enable or t_{WHAX} from Write Enable prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$, a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

Figure 7. Write Enable Controlled, Write AC Waveforms

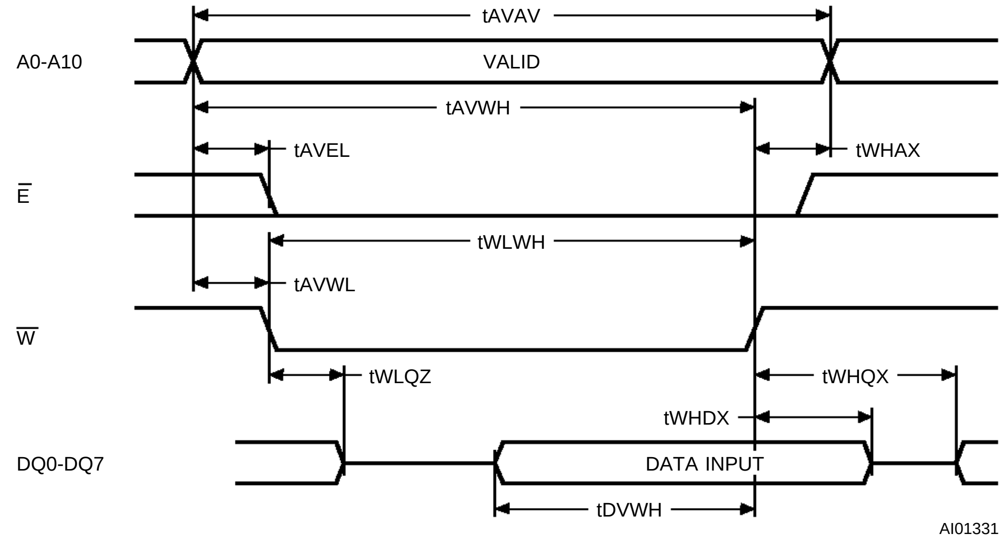
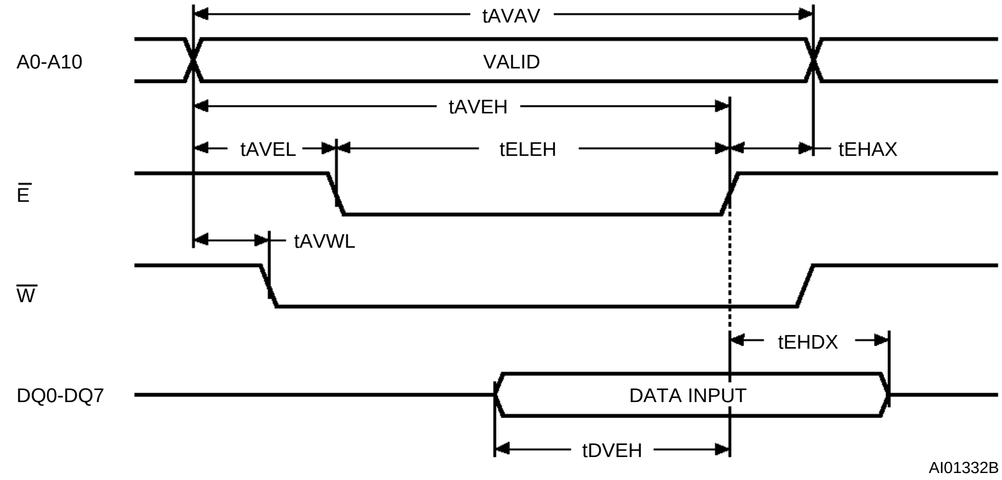


Figure 8. Chip Enable Controlled, Write AC Waveforms



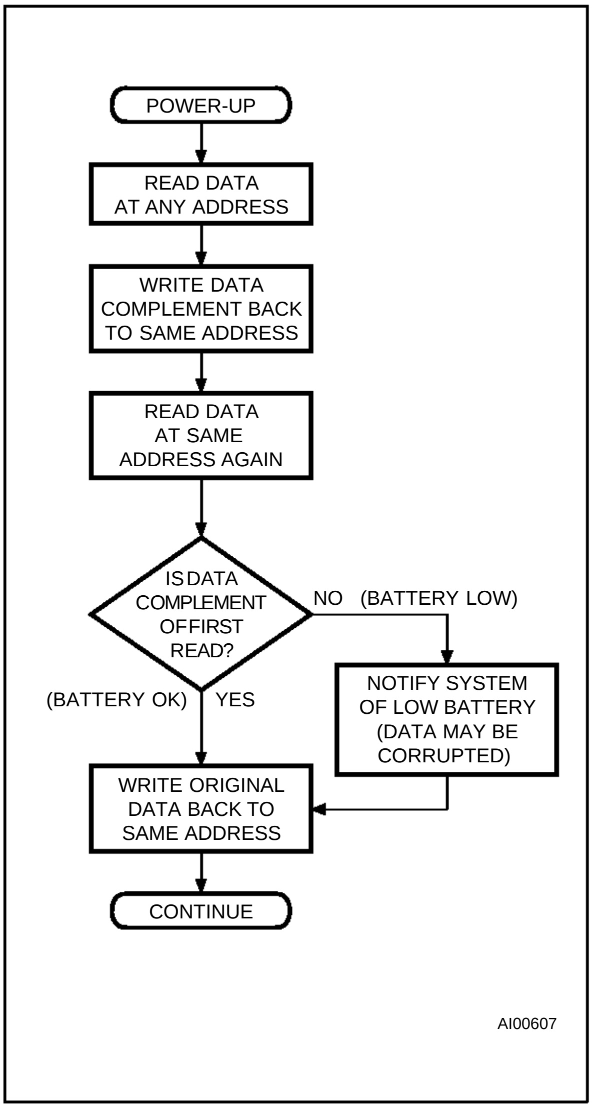
DATA RETENTION MODE

With valid V_{CC} applied, the M48Z02,12 operates as a conventional BYTEWIDE^{TM} static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD}(max), V_{PFD}(min) window. All outputs become high impedance, and all inputs are treated as ”don’t care.”

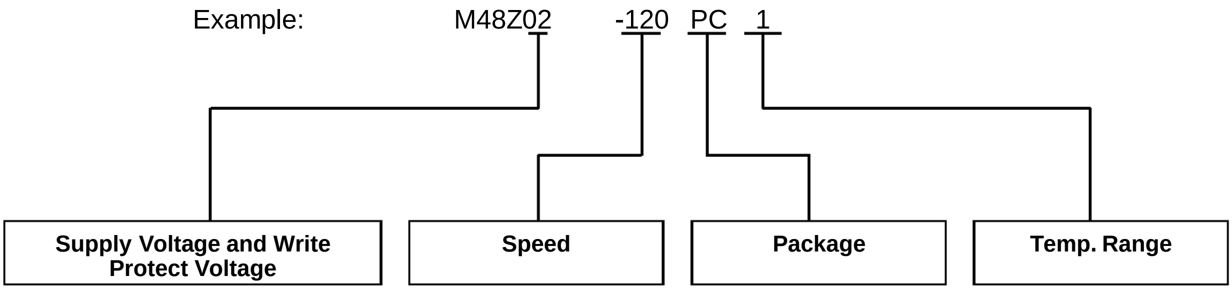
Note: A power failure during a write cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM’s content. At voltages below V_{PFD}(min), the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The M48Z02,12 may respond to transient noise spikes on V_{CC} that reach into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended.

The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. As V_{CC} rises, the battery voltage is checked. If the voltage is too low, an internal Battery Not OK ($\overline{\text{BOK}}$) flag will be set. The $\overline{\text{BOK}}$ flag can be checked after power up. If the $\overline{\text{BOK}}$ flag is set, the first write attempted will be blocked. The flag is automatically cleared after the first write, and normal RAM operation resumes. Figure 9 illustrates how a $\overline{\text{BOK}}$ check routine could be structured.

Figure 9. Checking the $\overline{\text{BOK}}$ Flag Status



ORDERING INFORMATION SCHEME



Supply Voltage and Write Protect Voltage		Speed		Package		Temp. Range	
02	V_{CC} = 4.75V to 5.5V V_{PFD} = 4.5V to 4.75V	-120	120ns	PC	PCDIP24	1	0 to 70 °C
12	V_{CC} = 4.5V to 5.5V V_{PFD} = 4.2V to 4.5V	-150	150ns			6	–40 to 85 °C
		-200	200ns				

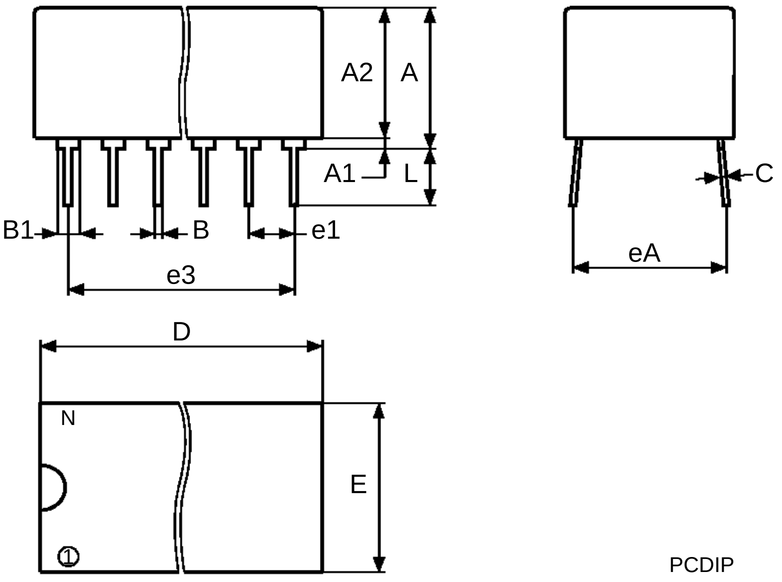
For a list of available options (Supply Voltage, Speed, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PCDIP24 - 24 pin Plastic DIP, battery CAPHAT

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		8.89	9.65		0.350	0.380
A1		0.38	0.76		0.015	0.030
A2		8.36	8.89		0.329	0.350
B		0.38	0.53		0.015	0.021
B1		1.14	1.78		0.045	0.070
C		0.20	0.31		0.008	0.012
D		34.29	34.80		1.350	1.370
E		17.83	18.34		0.702	0.722
e1		2.29	2.79		0.090	0.110
e3		25.15	30.73		0.990	1.210
eA		15.24	16.00		0.600	0.630
L		3.05	3.81		0.120	0.150
N	24			24		

PCDIP24



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